ZL30112
SLIC/CODEC DPLL

Data Sheet

November 2009

Features

- Synchronizes to 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz input
- Provides 2.048 MHz and 8.192 MHz output clocks and an 8 kHz framing pulse
- Automatic entry and exit from freerun mode on reference fail
- Provides DPLL lock and reference fail indication
- DPLL bandwidth of 29 Hz for all rates of input references
- Less than 0.6 $nsec_{pp}$ intrinsic jitter on all output clocks
- 20 MHz external master clock source: clock oscillator or crystal
- Simple hardware control interface

Applications

- Synchronizer for POTS SLIC/CODEC
- Rate convert NTR 8 kHz or GPON physical interface clock to TDM clock

Ordering Information

ZL30112LDG1	32 Pin QFN*	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Description

The ZL30112 SLIC/CODEC DPLL contains a digital phase-locked loop (DPLL), which provides timing and synchronization for SLIC/CODEC devices.

The ZL30112 generates TDM clock and framing signals that are phase locked to the input reference. It helps ensure system reliability by monitoring its reference for stability and by maintaining stable output clocks during short periods when the reference is unavailable.

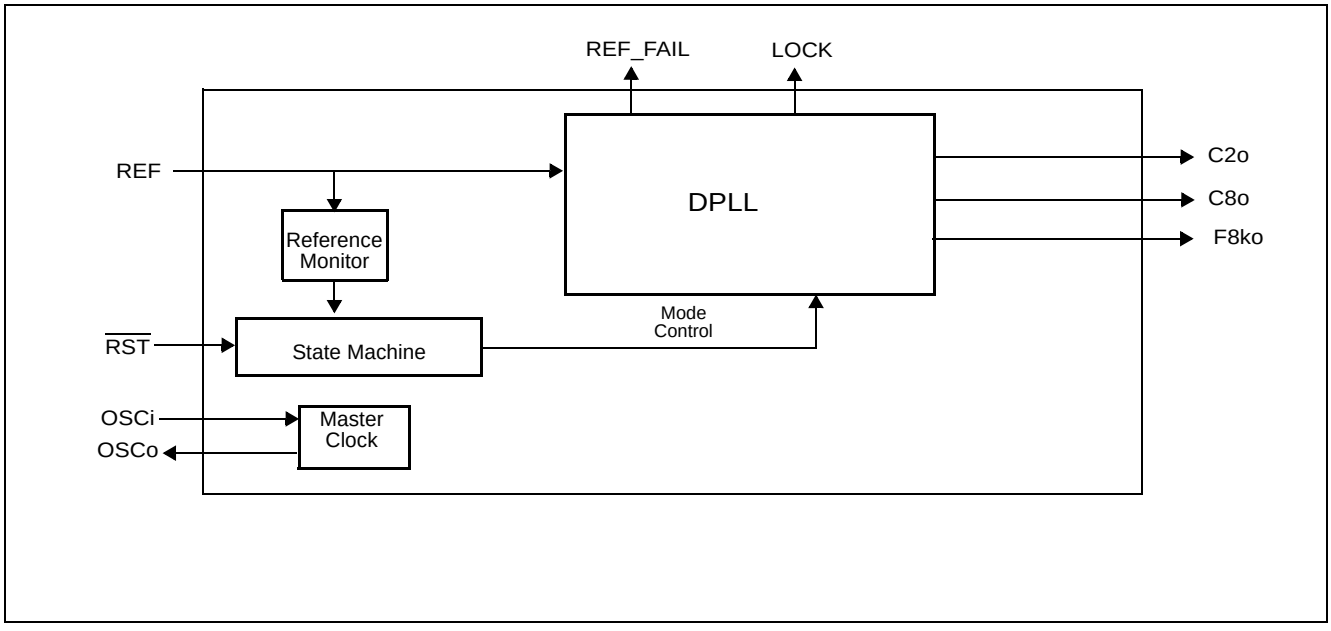

Figure 1 - Functional Block Diagram

1.0 Change Summary

Changes from November 2007 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information	Updates to Ordering Information and Package Drawing.

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2.0 Physical Description

2.1 Pin Connections

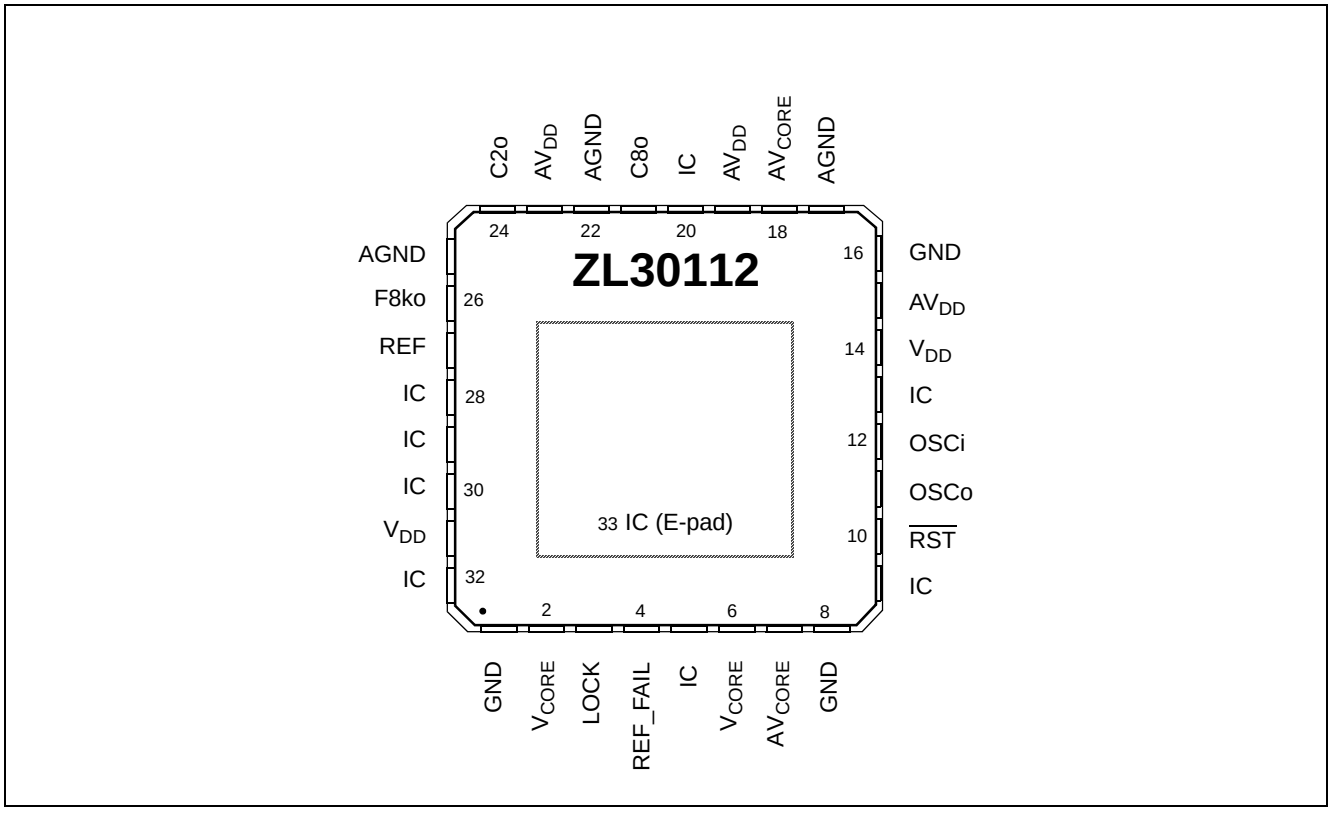


Figure 2 - Pin Connections (32 pin 5 mm X 5 mm QFN)

3.0 Pin Description

Pin #	Name	I/O Type	Description
1	GND		**Ground.** 0 V.
2	V_{CORE}		**Positive Supply Voltage.** +1.8 V_{DC} nominal.
3	LOCK	O	**Lock Indicator (LVCMOS).** This output goes to a logic high when the PLL is locked to a valid input reference.
4	REF_FAIL	O	**Reference Failure Indicator (LVCMOS).** A logic high at this output indicates that the REF input has failed.
5	IC	O	**Internal Connection.** Leave unconnected.
6	V_{CORE}		**Positive Supply Voltage.** +1.8 V_{DC} nominal.
7	AV_{CORE}		**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
8	GND		**Ground.** 0 V.
9	IC	I	**Internal Connection.** Connect to GND.
10	$\overline{RST}$	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. On power up, the $\overline{RST}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the $\overline{RST}$ pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all outputs will be forced into high impedance.
11	OSCo	O	**Oscillator Master Clock (LVCMOS).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.
12	OSCi	I	**Oscillator Master Clock (Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.
13	IC	I	**Internal Connection.** Connect to GND.
14	V_{DD}		**Positive Supply Voltage.** +3.3 V_{DC} nominal.
15	AV_{DD}		**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
16	GND		**Ground.** 0 V.
17	AGND		**Analog Ground.** 0V.
18	AV_{CORE}		**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
19	AV_{DD}		**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
20	IC	I	**Internal Connection.** Leave unconnected.
21	C8o	O	**Clock 8.192 MHz (LVCMOS).** This is a 8.192 MHz clock output.
22	AGND		**Analog Ground.** 0V.
23	AV_{DD}		**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
24	C2o	O	**Clock 2.048 MHz (LVCMOS).** This is a 2.048 MHz clock output.
25	AGND		**Analog Ground.** 0V.
26	F8ko	O	**Frame Pulse (LVCMOS).** This is an 8 kHz frame pulse which marks the beginning of a 125 us frame. Pulse width is 122 ns.

Pin #	Name	I/O Type	Description
27	REF	I	**Reference Input.** This input is used to synchronize the PLL. Synchronizes to 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz.
28	IC	I	**Internal Connection.** Leave unconnected.
29	IC	I	**Internal Connection.** Connect to VDD.
30	IC	I	**Internal Connection.** Connect to VDD.
31	V_{DD}		**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
32	IC	I	**Internal Connection.** Connect to GND.
33	GND		**Ground.** 0 V. Package E-pad. This pin is internally connected to device GND. It must be externally connected to GND.

4.0 Functional Description

The ZL30112 is a SLIC/CODEC DPLL providing timing (clock) and synchronization (frame) signals to network interface cards. Figure 1 is a functional block diagram which is described in the following sections.

4.1 Reference Monitor

The input reference is monitored by two reference monitor blocks. The block diagram of reference monitoring is shown in Figure 3. The reference frequency is detected and the clock is continuously monitored for two independent criteria that indicate abnormal behavior of the reference signal, for example; loss of clock or excessive level of frequency error. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference frequency over intervals of approximately 30 μs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

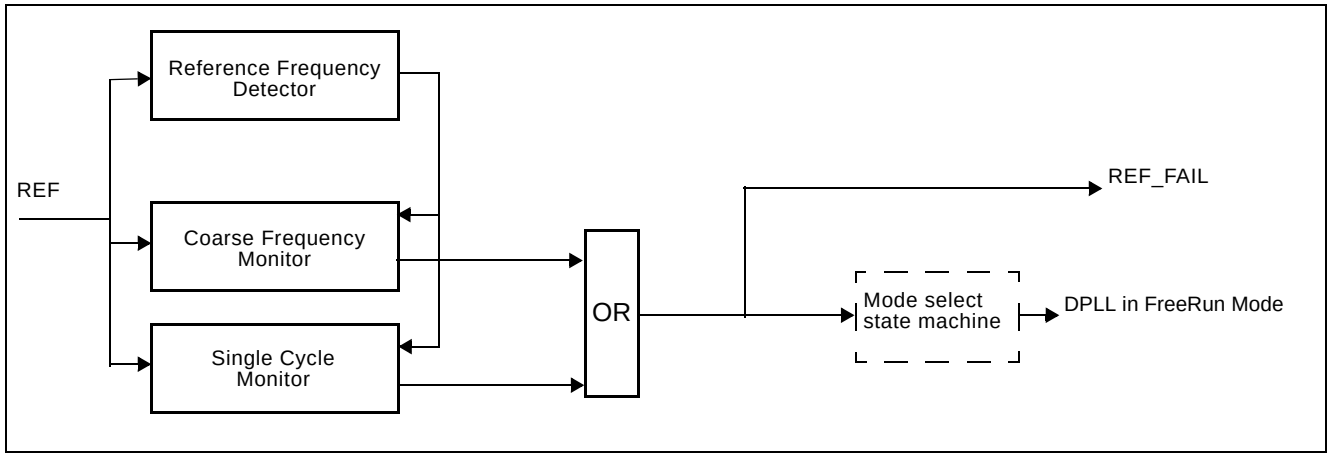


Figure 3 - Reference Monitor Circuit

Exceeding the thresholds of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into FreeRun mode.

4.2 Time Interval Error (TIE) Corrector Circuit

The TIE Corrector Circuit eliminates phase transients on the output clock that may occur in the course of recovery from Automatic Freerun mode to Normal mode.

On recovery from Automatic Freerun mode, the TIE corrector circuit measures the phase delay between the current phase (feedback signal) and the phase of the selected reference signal. This delay value is stored in the TIE corrector circuit. This circuit creates a new virtual reference signal that is at the same phase position as the feedback signal. By using the virtual reference, the PLL minimizes the phase transient it experiences when it switches to another reference input or recovers from Automatic Freerun mode.

4.3 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30112 consists of a phase detector, an integrated on-chip loop filter, and a digitally controlled oscillator as shown in Figure 4. The data path from the phase detector to the filter is tapped and routed to the lock indicator that provides a lock indication which is output at the LOCK pin.

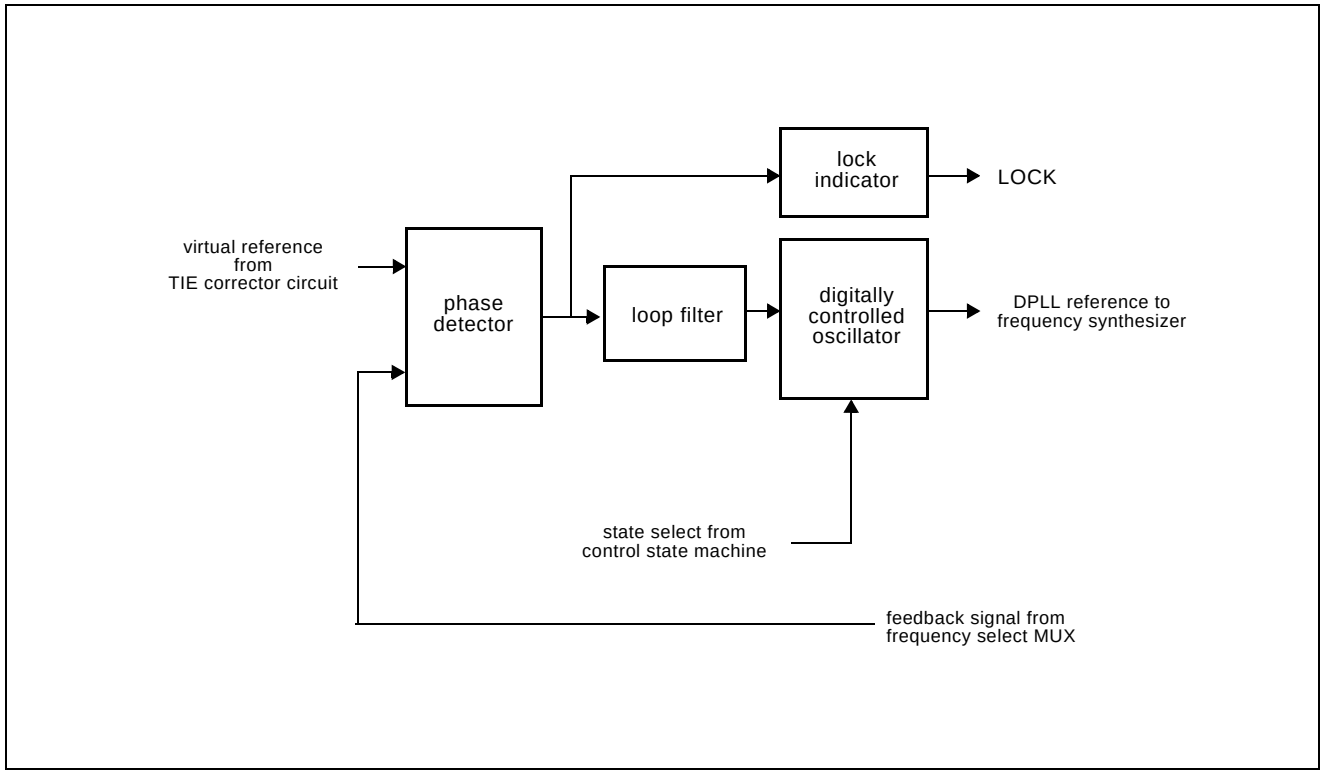


Figure 4 - DPLL Block Diagram

Phase Detector - the phase detector compares the virtual reference signal from the TIE corrector circuit with the feedback signal and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the loop filter circuit.

Loop Filter - the loop filter is similar to a first order low pass filter with bandwidth of 29 Hz suitable to provide timing and synchronization for network interface cards.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30112.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In the Automatic Freerun mode, the DCO is free running at a frequency equal to the frequency that the DCO was generating in Normal Mode.

Lock Indicator - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into the Automatic Freerun mode, the LOCK pin will initially stay high for 0.1 s. If at that point the DPLL is still in the Automatic Freerun mode, the LOCK pin will go low.

4.4 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizers to generate the output clocks and frame pulses which are synchronized to the input reference (REF).

The frequency synthesizer uses digital techniques to generate output clocks and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited drive capability and should be buffered when driving high capacitance loads.

4.5 Master Clock

The ZL30112 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

5.0 Modes of Operation

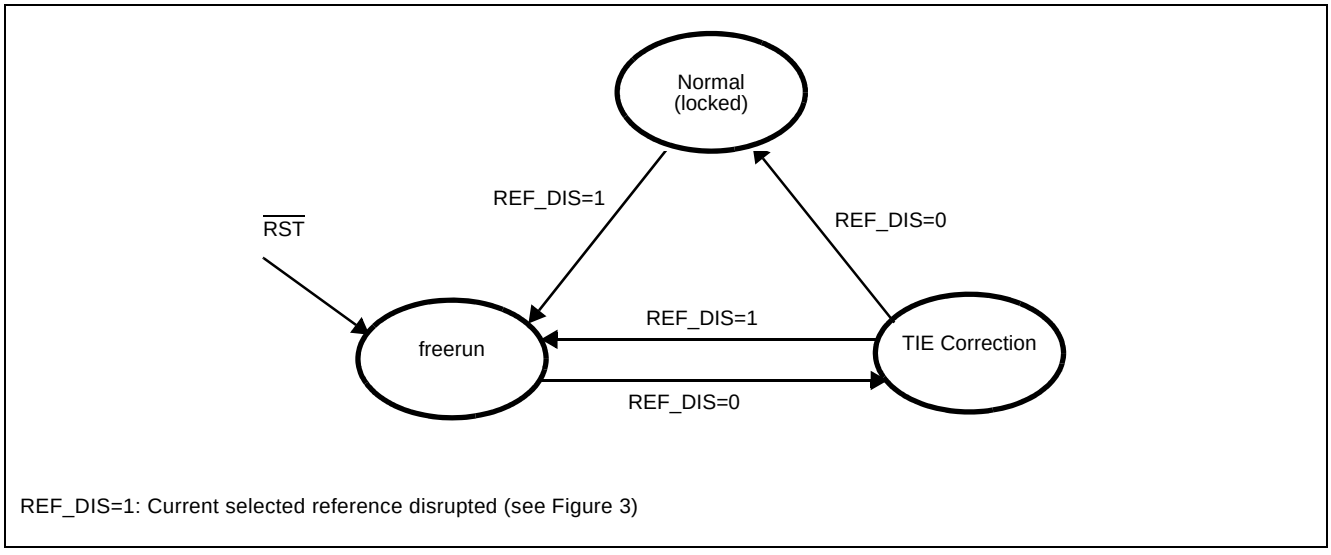


Figure 5 - Modes of Operation

Normal Mode

In Normal mode, the ZL30112 provides timing and frame synchronization signals which are synchronized to the reference input (REF). The input reference signal may have a nominal frequency of 8 kHz, 2.048 MHz, 8.192 MHz, or 19.44 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

Automatic Freerun Mode

Automatic freerun mode is typically used for short durations while system synchronization is temporarily disrupted.

In Automatic freerun mode, the ZL30112 provides timing and synchronization signals, which are not locked to an external reference signal, but are based on the freerun accuracy of the external oscillator.

6.0 Measures of Performance

The following are some PLL performance indicators and their corresponding definitions.

6.1 Jitter Generation (Intrinsic Jitter)

Timing jitter is defined as the high frequency variation of the clock edges from their ideal positions in time. Wander is defined as the low-frequency variation of the clock edges from their ideal positions in time. High and low frequency variation imply phase oscillation frequencies relative to some demarcation frequency. (Often 10 Hz or 20 Hz for DS1 or E1, higher for SONET/SDH clocks.) Jitter parameters given in this data sheet are total timing jitter numbers, not cycle-to-cycle jitter.

6.2 Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

6.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards. For the ZL30112, the internal low pass loop filter determines the jitter attenuation.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (for example 75% of the specified maximum tolerable input jitter).

6.4 Freerun Accuracy

Frequency accuracy is defined as the absolute accuracy of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the ZL30112, the Freerun accuracy is equal to the master clock (OSCi) accuracy.

6.5 Capture Range

Also referred to as pull-in range. This is the input frequency range over which the PLL must be able to pull into synchronization. The ZL30112 capture range is equal to $\pm$130 ppm minus the accuracy of the master clock (OSCi). For example, a +32 ppm master clock results in a capture range of +162 ppm on one side and -98 ppm on the other side of frequency range.

6.6 Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the ZL30112.

6.7 Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

6.8 Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

6.9 Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the PLL after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

6.10 Phase Lock Time

This is the time it takes the PLL to phase lock to the input signal. Phase lock occurs when the input signal and output signal are aligned in phase with respect to each other within a certain phase distance (not including jitter). Lock time is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- PLL loop filter bandwidth
- in-lock phase distance

The presence of input jitter makes it difficult to define when the PLL is locked as it may not be able to align its output to the input within the required phase distance, dependent on the PLL bandwidth and the input jitter amplitude and frequency.

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. See Section 8.2, “Performance Characteristics“ for Maximum Phase Lock Time.

7.0 Applications

This section contains ZL30112 application specific details for power supply decoupling, clock and crystal operation, reset operation, and control operation.

7.1 Power Supply Decoupling

Jitter levels on the ZL30112 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30112 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-178.

7.2 Master Clock

The ZL30112 can use either a clock or crystal as the master timing source. Zarlink Application Note ZLAN-68 lists a number of applicable oscillators and crystals that can be used with the ZL30112.

7.2.1 Clock Oscillator

When selecting a Clock Oscillator, numerous parameters must be considered. These includes absolute frequency, frequency change over temperature, output rise and fall times, output levels, duty cycle and phase noise.

1	Frequency	20 MHz
2	Tolerance	As required
3	Rise & Fall Time	<10 ns
4	Duty Cycle	40% to 60%

Table 1 - Typical Clock Oscillator Specification

The output clock should be connected directly (not AC coupled) to the OSCi input of the ZL30112 and the OSCo output should be left open as shown in Figure 6.

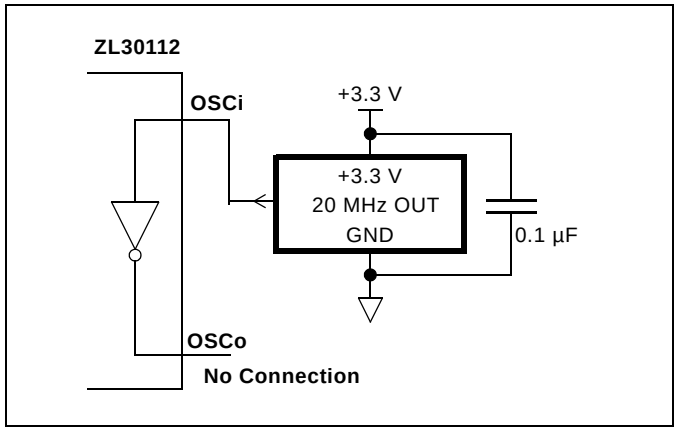


Figure 6 - Clock Oscillator Circuit

7.2.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 7.

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

1	Frequency	20 MHz
2	Tolerance	As required
3	Oscillation Mode	Fundamental
4	Resonance Mode	Parallel
5	Load Capacitance	As required
6	Maximum Series Resistance	50 Ω

Table 2 - Typical Crystal Oscillator Specification

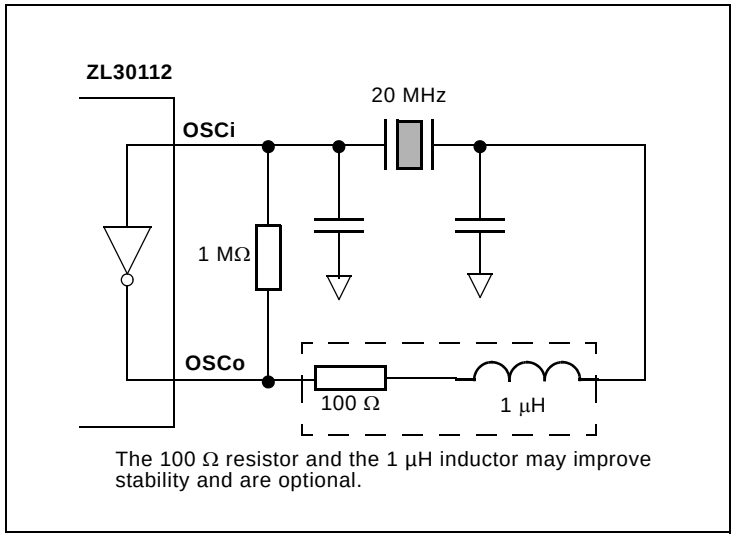


Figure 7 - Crystal Oscillator Circuit

7.3 Power Up Sequence

The ZL30112 requires that the 3.3 V is not powered after the 1.8 V. This is to prevent the risk of latch-up due to the presence of parasitic diodes in the IO pads.

Two options are given:

1. Power-up 3.3 V first, 1.8 V later
2. Power up 3.3 V and 1.8 V simultaneously ensuring that the 3.3 V power is never lower than 1.8 V minus a few hundred millivolts (e.g., by using a schottky diode or controlled slew rate)

7.4 Reset Circuit

A simple power up reset circuit with about a 60 µs reset low time is shown in Figure 8. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

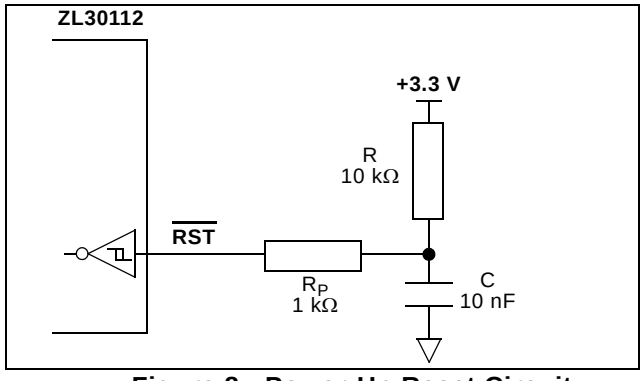


Figure 8 - Power-Up Reset Circuit

8.0 Characteristics

8.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on OSCi and OSCo pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Current on any pin	I_{PIN}		30	mA
6	Storage temperature	T_{ST}	-55	125	°C
7	Package power dissipation	P_{PD}		195	mW
8	ESD rating	V_{ESD}		2k	V

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	2.97	3.30	3.63	V
2	Core supply voltage	V_{CORE}	1.62	1.80	1.98	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Supply current with: OSCi = 0 V	I_{DDS}	2.5	7.0	mA	Outputs loaded with 30 pf
2	OSCi = Clock	I_{DD}		43	mA	Outputs unloaded
3	Core supply current with: OSCi = 0 V	I_{CORES}		20	uA	
4	OSCi = Clock	I_{CORES}		18	mA	
5	Schmitt trigger Low to High threshold point	V_{CIH}	1.43	1.85	V	All device inputs are Schmitt trigger type.
6	Schmitt trigger High to Low threshold point	V_{CIL}	0.8	1.1	V	
7	Input leakage current	I_{IL}	-105	105	µA	V_I=V_{DD} or 0 V

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
8	High-level output voltage	V_{OH}	2.4		V	I_{OH} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs
9	Low-level output voltage	V_{OL}		0.4	V	I_{OL} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Timing Parameter Measurement Voltage Levels (see Figure 9).

	Characteristics	Sym.	CMOS	Units
1	Threshold Voltage	V_T	1.5	V
2	Rise and Fall Threshold Voltage High	V_{HM}	2.0	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	0.8	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

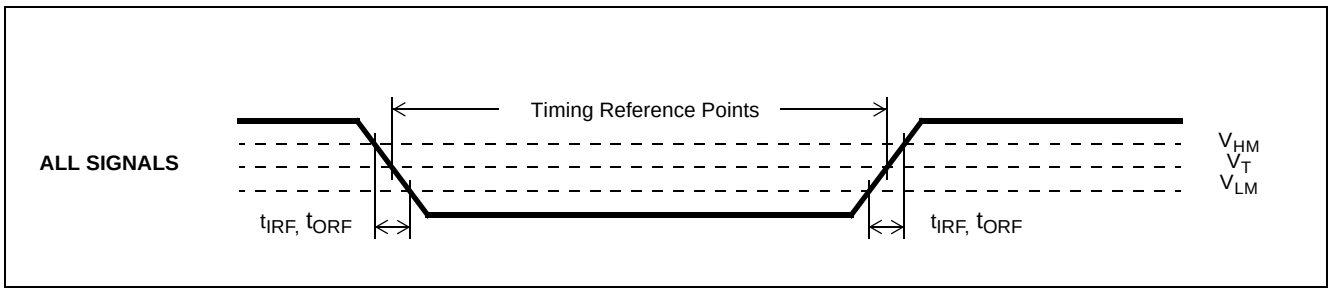


Figure 9 - Timing Parameter Measurement Voltage Levels.

AC Electrical Characteristics* - Input timing reference REF (see Figure 11).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	8 kHz reference period	t_{REF8kP}	120	125	128	µs
2	2.048 MHz reference period	t_{REF2P}	263	488	712	ns
3	8.192 MHz reference period	t_{REF8P}	63	122	175	ns
4	19.44 MHz reference period	t_{REF8kP}	38	51	75	ns
5	Reference pulse width high or low	t_{REFW}	15			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Period Min/Max values are the limits to avoid a single-cycle fault detection. Short-term and long-term average periods must be within Out-of-Range limits.

AC Electrical Characteristics* - Output Timing (see Figure 10)

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	F8o pulse width high	t_{F8H}	121	124	ns	
2	C2o pulse width low	t_{C2L}	243	245	ns	
3	C2o delay	t_{C2D}	-1.0	1.0	ns	
4	C8o pulse width low	t_{C8L}	60	62	ns	
5	C8o delay	t_{C8D}	-1.0	1.0	ns	
6	Output clock and frame pulse rise time	t_{OR}	1.0	2.0	ns	
7	Output clock and frame pulse fall time	t_{OF}	1.0	2.5	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions and 30 pF load.

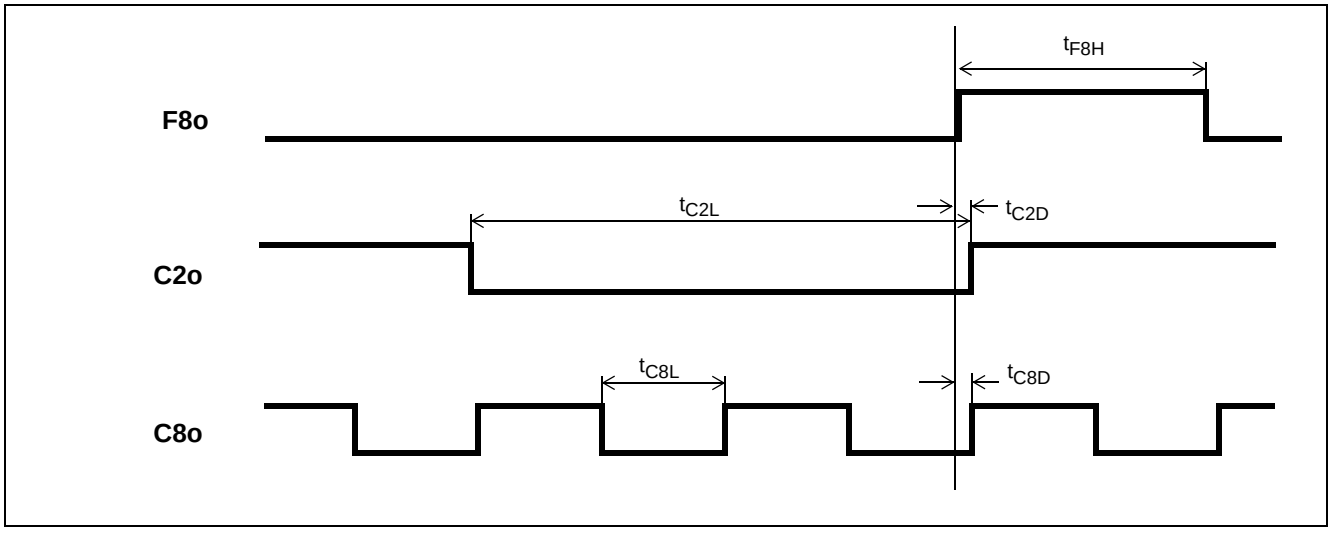


Figure 10 - Output Timing Referenced to F8o

AC Electrical Characteristics* - Input to output timing for reference REF (see Figure 11).

	Characteristics	Symbol	Min.	Max.	Units
1	8 kHz reference input to F8ko delay	t_{REF8kD}	-0.3	2	ns
2	2.048 MHz reference input to F8ko delay	t_{REF2_F8kD}	-1.1	0.9	ns
3	8.192 MHz reference input to F8ko delay	t_{REF8_F8kD}	-0.6	0.8	ns
4	19.44 MHz reference input to F8ko delay	t_{REF19_F8kD}	-1.7	1	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

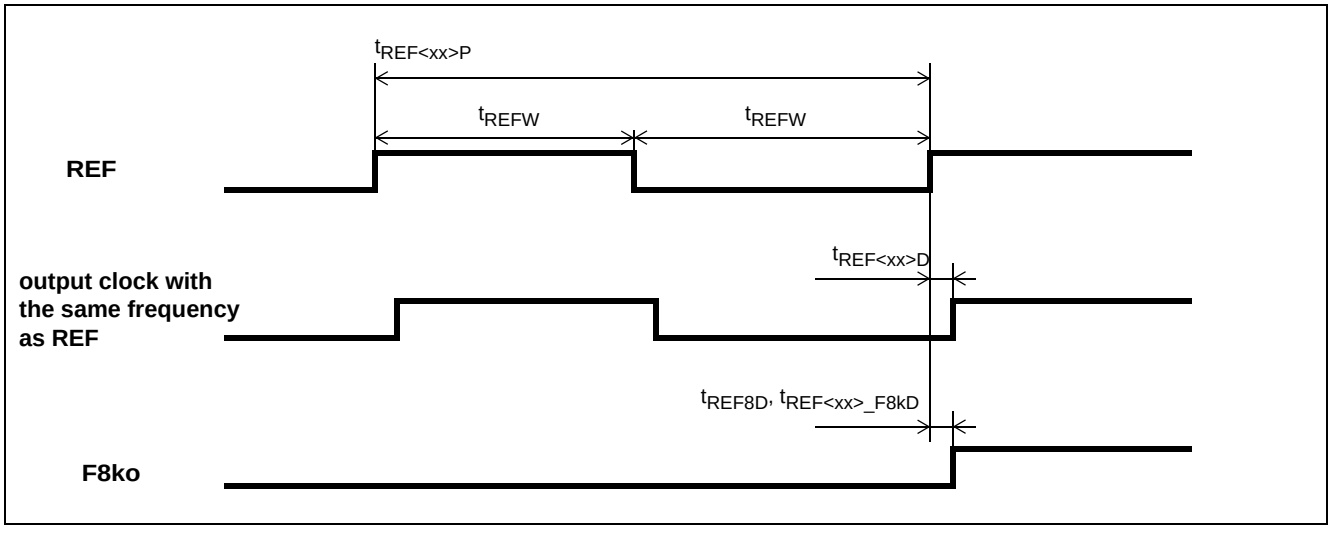


Figure 11 - Input to Output Timing

AC Electrical Characteristics* - OSCi 20 MHz Master Clock Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Oscillator Tolerance		-32		+32	ppm	
2	Duty cycle		40		60	%	
3	Rise time				10	ns	
4	Fall time				10	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

8.2 Performance Characteristics

Performance Characteristics* - Functional

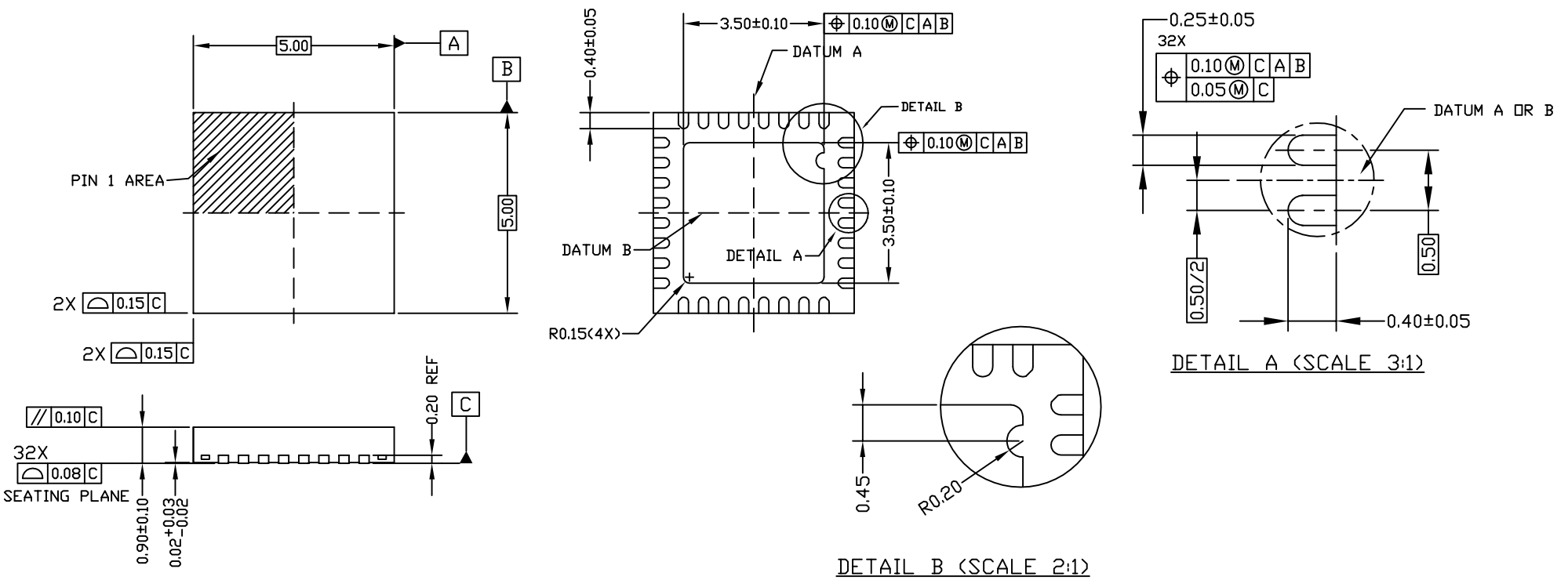
	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Freerun stability		NA		ppm	Determined by stability of the 20 MHz Master Clock oscillator
2	Capture range	-130		+130	ppm	The 20 MHz Master Clock oscillator set at 0.ppm
Lock Time**						
3	29 Hz Filter			1	s	
Output Phase Continuity (MTIE)						
4	Switching from Normal mode to Automatic Freerun mode		0		ns	
5	Switching from Automatic Freerun mode to Normal mode		13		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
** Lock Time represent time to achieve phase/frequency lock and it excludes time to pull-in the input to output phase difference.

Performance Characteristics* - Unfiltered Intrinsic Jitter

	Signal	Max. [ns_{pp}]	Notes
1	C2o	0.6	
2	C8o	0.6	
3	F8ko (8 kHz)	0.6	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



DETAIL B (SCALE 2:1)

DETAIL A (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Zarlink Semiconductor				DWG. NO.	REV.
TITLE 32 QFN PACKAGE OUTLINE BODY SIZE : 5X5X0.90 mm PITCH : 0.50mm				CDCA 22–0005 ASE84–06–137–167	1
				SHEET: 1 OF 1	SIZE: A0
BY	DRAWN	CHECKED	APPROVED	ACAD FILE	REF JEDEC NO
	ASE	J Kelly	J Kelly	D6137167	MO–220

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